THAT WHICH IS CLAIMED IS:

1. A method of reading a capacitive sensor constituted by an array of capacitors ordered in rows and columns functionally connected through row lines, each electrically constituting a first plate of all the capacitors of a row, and through column lines, each electrically constituting a second plate of all the capacitors of a column, orthogonal or quasi-orthogonal to each other, using a biasing and reading circuit (READOUT) comprising column and row selectors, a charge amplifier outputting a voltage (V_o) function of the capacitance of a selected capacitor (C_{PIX}) of said array, comprising the steps of:

preliminarily resetting the output voltage (V_o) of said charge amplifier;

connecting to a reference voltage all the deselected row and column plates of said array and connecting an auxiliary capacitor (C_R) and said selected capacitor (Cpix) to an inverting input (-) of the amplifier and as feedback capacitor of said amplifier, respectively, or viceversa;

applying a step voltage (V_I) on the capacitor (C_R, C_{PIX}) that is connected to the inverting input (-) of the amplifier and reading at steady-state, said output voltage (V_o).

2. The method of claim 1, wherein the reading of the sensor includes a sequential scanning of the capacitors of the array, obtaining a frame of as many values of capacitance of the sensor.

3. The method of claim 2, wherein the scan is repeated with a certain frame frequency.

4. An integrated system for reading a capacitive sensor constituted by an array of capacitors

ordered in rows and columns functionally connected through row lines, each electrically constituting a first plate of all the capacitors of a row, and through column lines, each electrically constituting a second plate of all the capacitors of a column, orthogonal or quasi-orthogonal to each other, comprising:

an input interface circuit (ANAIO) for coupling therethrough said capacitive sensor, the interface circuit grounding deselected row plates and column plates of said array and connecting a single capacitor (C_{PIX}) at the time selected by row and column selectors;

a biasing and reading circuit (READOUT) composed of a charge amplifier outputting said voltage (V_o) function of the capacitance of the selected capacitor (C_{PIX}), having an inverting input (-), a feedback capacitor and a reset switch (S1), configuration switches for coupling said auxiliary capacitor (C_R) and said selected capacitor (Cpix) as feedback capacitor and to said input of the amplifier, respectively or viceversa;

an analog-to-digital converter (ADC) converting said output voltage (V_o) in a corresponding multibit datum;

a processing and controlling microprocessor unit (COMPUTING CORE) performing noise filtering and real-time correction of data;

a digital output interface circuit (DIGITALI/O) controlled by said microprocessor unit for outputting the data of the read values of capacitance of the sensor.

5. The system according to claim 4, further comprising a timing signal generator (WAVEFORM GENERATOR), controlled by said microprocessor unit, generating timing signals for said row and column selectors, for the biasing and reading circuit (READOUT) and for the

converter (ADC), for synchronizing the operation phases of the circuits.

6. The system of claim 5, wherein said waveform generator (WAVEFORM GENERATOR) is composed of a

a shift register cyclically producing said timing signals with a certain frequency;

a finite state machine, controlled by the microprocessor unit, for configuring said shift register.

7. The system according to any of claims from 4 to 6, wherein said input interface circuit (ANAIO) comprises

a plurality of identical connection modules (ANAIOCIRCUIT) for grounding the deselected row plates and the deselected column plates, and coupling to said biasing and reading circuit (READOUT) the selected capacitor (C_{PIX}), in function of selection signals (ISIN, SELTHIS);

a selection logic circuit (ANAIOCONTROL) controlled by said microprocessor unit (COMPUTING CORE) producing said selection signals (ISIN, SELTHIS).